AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A fault tolerant computer comprising:

~~a plurality of~~ first and second CPU (Central Processing Unit) modules processing the same instruction string while maintaining clock synchronization;

~~a plurality of I/O modules~~ an I/O module ~~each~~ having a plurality of device controllers each executing input/output control processing for a device; and

a plurality of transaction synchronization controllers, ~~provided in each of said device controllers, that checks if sequences of I/O transactions issued from said plurality of CPU modules match and, if the sequences match, judges that an out-of-synchronization condition is not caused.~~each of which is provided with corresponding one of said device controllers, checks if first and second sequences of I/O transactions addressed to said corresponding device controller issued from said first and second CPU modules, respectively, match, and determines whether out-of-synchronization occurs.

2. (currently amended): The fault tolerant computer according to claim 1, wherein said transaction synchronization controller comprises:

a timer ~~means for measuring~~ element which measures a predetermined time; and

a comparison ~~means for checking if the sequences of I/O transactions, issued from the plurality of CPU modules, match on a device controller basis~~ element which checks if said first and second sequences match while waiting for the predetermined time.

3. (currently amended): The fault tolerant computer according to claim 2, wherein said transaction synchronization controller further comprises an output controller that outputs said I/O transactions to said device controller when said first and second sequences match.

4. (currently amended): The fault tolerant computer according to claim 3, wherein, when the I/O transactions from the first and second CPU modules match, said output controller outputs the matching I/O transactions to said device controller, one at a time.

5. (currently amended): The fault tolerant computer according to claim 2, wherein, when the first and second sequences do not match within the predetermined time or when the first and second sequences of I/O transactions differ, said output controller outputs a failure notification.

6. (currently amended): The fault tolerant computer according to claim 2, ~~further comprising a plurality of storage means~~ wherein said transaction synchronization controller further comprises first and second storage elements in which the I/O transactions issued from said ~~plurality of~~ first and second CPU modules are stored.

7. (currently amended): The fault tolerant computer according to claim ~~2~~6, wherein said transaction synchronization controller further comprises selection circuits ~~that~~ which select between said ~~plurality of storage means and said CPU modules~~ first storage element and said first CPU module and which select between said second storage element and said second CPU module, as a source from which I/O transactions to be sent to said comparison ~~means~~ element are received.

8. (currently amended): A transaction synchronization control method for use in a fault tolerant computer, said method comprising:

~~a first step of~~ sending a plurality of, and the same, I/O transactions from ~~a plurality of~~ first and second CPU modules, which process the same instruction string while maintaining clock synchronization, to a plurality of device controllers in an I/O module; and

~~a second step of~~ checking if first and second sequences of ~~the received~~ I/O transactions addressed to said device controller issued from said first and second CPU modules, respectively, match and determining whether out-of synchronization occurs. ~~in each of a plurality of device controllers provided in said I/O module and, if the sequences match, judging that an out-of-synchronization condition is not caused.~~

9. (currently amended): The transaction synchronization control method according to claim 8, wherein said ~~second~~ checking step checks if ~~the~~ said first and second sequences of I/O transactions match while waiting for a predetermined time.

10. (currently amended): The transaction synchronization control method according to claim 9, further comprising ~~a third step of~~ outputting the I/O transactions to said device controller when ~~the~~ said first and second sequences match.

11. (currently amended): The transaction synchronization control method according to claim 9, wherein, for each device controller, said ~~first~~ sending step stores the I/O transactions issued from said ~~plurality of~~ first and second CPU modules into ~~a plurality of~~ first and second storage ~~means~~ elements, respectively and

wherein said ~~second~~ checking step sends the I/O transactions, stored in said first and second storage elements ~~received from the CPU modules~~, to comparison ~~means~~ element which checks if said first and second sequences match ~~for use in comparing the I/O transactions~~, checks if the predetermined time has elapsed if ~~the I/O transactions~~ said first and second sequences do not match, and ~~judges~~ determines that an out-of-synchronization condition is not caused if the predetermined time has not yet elapsed.

12. (currently amended): The transaction synchronization control method according to claim 11, wherein, when the received I/O transactions match, the matching I/O transactions are output to said device controller, one at a time.

13. (currently amended): The transaction synchronization control method according to claim 9, further comprising ~~the step of~~ outputting a failure notification when ~~the~~ said first and second sequences do not match within the predetermined time.

14. (currently amended): The transaction synchronization control method according to claim 11, further comprising ~~the step of~~ selecting between said ~~plurality of~~ storage ~~means~~ element and said first CPU ~~modules~~ module and selecting between said second storage element and said second CPU model, as a source when a new I/O transaction is sent to said comparison ~~means~~ element.

15. (currently amended): The transaction synchronization control method according to claim 14, wherein, when ~~the~~ said first and second storage ~~means~~ elements do not contain effective data, said ~~step of~~ selecting step ~~between said plurality of storage means and said CPU modules~~ switches the source to ~~the~~ first and second CPU modules, respectively.

16. (currently amended): ~~A transaction synchronization control program product for use in a fault tolerant computer in which the same instruction string is processed by a plurality of CPU modules while maintaining clock synchronization, said program product~~ A computer program product having a computer readable medium with computer readable program code stored thereon, said computer readable code comprising the steps of:

~~a first step of~~ sending a plurality of, and the same, I/O transactions from ~~the plurality of~~ first and second CPU modules to a plurality of device controller in an I/O module; and

~~a second step of~~ checking if first and second sequences of ~~the received~~ I/O transactions addressed to said device controller issued from said first and second CPU modules, respectively, match and determining whether out-of-synchronization occurs. ~~in each of a plurality of device~~

~~controllers provided in said I/O module and, if the sequences match, judging that an out-of-synchronization condition is not caused~~.

17. (currently amended): The ~~transaction synchronization control~~ program product according to claim 16, wherein said ~~second~~ checking step checks if ~~the~~ said first and second sequences of I/O transactions match while waiting for a predetermined time.

18. (currently amended): The ~~transaction synchronization control~~ computer program product according to claim 17, further comprising ~~a third step of~~ outputting the I/O transactions to said device controller when ~~the~~ said first and second sequences match.

19. (currently amended): The ~~transaction synchronization control~~ computer program product according to claim 16, further comprising ~~the step of~~ outputting a failure notification when ~~the~~ said first and second sequences do not match within the predetermined time or when ~~the~~ first and second sequences of I/O transactions differ.

20. (currently amended): The ~~transaction synchronization control~~ computer program product according to claim 17,

wherein, for each device controller, said ~~first~~ sending step comprises ~~the step of~~ storing the I/O transactions, issued from said ~~plurality of~~ first and second CPU modules, into ~~a plurality of~~ first and second storage ~~means~~ elements, respectively and

wherein said ~~second~~ checking step comprises ~~the steps of~~ sending the I/O transactions ~~received from the CPU modules~~ stored in said first and second storage element to comparison ~~means~~ element which checks if said first and second sequences match and comparing the I/O transactions; checking if the predetermined time has elapsed if ~~the I/O transactions~~ said first and second sequences do not match; and ~~judging~~ determining that an out-of-synchronization condition is not caused when the predetermined time has not yet elapsed.